Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

1. (Currently amended) A method comprising:

generating an expected parity for data before loading the data into a cache;

fetching ~~data from a cache in a computer~~ the data from the cache;

~~during the fetching, detecting a soft error in the data;~~

calculating a parity for the fetched data;

comparing the expected parity with the calculated parity;

detecting a soft error in the fetched data based on the comparing;

as a result of detecting the soft error, stalling the computer;

invoking soft error handler logic to perform one of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache;

and

resuming fetching of the data.

2. - 5. (Canceled)

6. (Currently amended) A system comprising:

a memory;

a processor coupled to the memory;

a cache coupled to the processor;

soft error detection logic coupled to the cache to detect soft errors therein, the soft error detection logic to detect a soft error based on comparing an expected parity with a calculated parity, the expected parity being generated for data before loading the data into the cache, and the calculated parity being calculated for the data while the data is fetched from the cache;

soft error handling decision logic coupled to the soft error detection logic to invoke soft error handler logic based on an input from the soft error detection logic; and

soft error handler logic to perform one of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache.

7. (Canceled)

8. (Original) The system of claim 6, further comprising a soft error recovery memory to store information associated with recovering from a soft error.

9. (Original) The system of claim 8, wherein the information is an address of a cache line containing a soft error.

10. (Original) The system of claim 8, wherein the soft error recovery memory comprises a register.

11. (Canceled)

12. (Original) The system of claim 6, wherein the soft error handling decision logic comprises a multiplexer configured to select as input one of data corresponding to a cache line currently being fetched and a request to invoke the soft error handler, depending on a value of an output of the soft error detection logic.

13. (Currently amended) A processor comprising:

a cache;

soft error detection logic coupled to the cache;

decision logic to receive at least first, second and third input values, the first input value being a request to invoke a soft error handler, the second input value corresponding to data in a cache line of the ~~instruction~~ cache, and the third input value being an indicator from the soft error detection logic to indicate whether a soft error is present in the data in the cache line, the soft error detection logic to detect a soft error based on comparing an expected parity with a calculated parity, the expected parity being generated for data before loading the data into the cache, and the calculated parity being calculated for the data while the data is fetched from the cache; and

soft error handler logic to perform one of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache.

14. (Previously presented) The processor of claim 13, further comprising a register to store an address of a cache line containing data currently being fetched.

15. – 16. (Canceled)

17. (Currently amended) The method of claim 1, further comprising:

after detecting the soft error, storing the address of ~~the~~ a cache line corresponding to the ~~at least one instruction~~ soft error in a register~~; and~~

~~issuing a request to a soft error handler to clear the soft error~~.

18. (Currently amended) The method of claim 17, wherein the soft error handler logic:

stops fetching of a sequence of computer instructions from the cache;

reads the address in the register; and

clears the corresponding cache line.

19. (Currently amended) The method of claim ~~17~~ 18, further comprising resuming execution of the sequence of computer instructions at the instruction corresponding to the cleared cache line.

20. (Previously presented) A machine-readable medium storing computer-executable instructions which, when executed by a processor, implement a process according to claim 1.

21. (Previously presented) The machine-readable medium of claim 20, the process further including reading a memory storing an address of the cache line.

22. (Previously presented) The machine-readable medium of claim 20, the process further including invalidating the cache line.

23. (Currently amended) An apparatus comprising:

a cache;

a comparator coupled to the cache to compare a calculated parity bit and an expected parity bit, the expected parity bit being generated for data before loading the data into the cache, and the calculated parity bit being calculated for the data while the data is fetched from the cache, the comparator including an output coupled to an enable input of a recovery register, the enable input to cause the recovery register to store an address of a cache line identified as containing a soft error; and

a selector coupled to the cache line, to select one of a soft error handler request or the cache line based on the comparator output, the soft error handler request to invoke a soft error handler, the soft error handler to receive the address of the cache line identified as containing a soft error from the recovery register, and to perform one of multiple possible operations to clear the soft error, the multiple possible operations including one of flushing the cache, invalidating a cache line, and clearing an intermediate portion of the cache.

24. (Previously presented) The apparatus of claim 23, wherein the soft error handler comprises microcode.